WHAT IS CLAIMED IS:

1. A data processing apparatus comprising:

a processor;

an input device for supplying input information to be processed, said input information including probability bittors indicating uncertainty of correctness;

a storage media containing rules for manipulating said input information to yield output information, said rules being capable of processing said bittors; and

an output device for receiving said output information from said processor.

2. A data processing apparatus as set forth in claim 1, wherein said probability bittors contain an order collection of numbers indicating truth and falsity, respectively.

3. A data processing apparatus as set forth in claim 2, wherein said rules for manipulating include logical operations.

4. A data processing apparatus as set forth in claim 3, wherein said logical operations function according to the equation $z_i = c^t_{ijk} x_j\, y_k$, where z_i is a bittor resulting from application of logical operation c^t_{ijk} on bittors x_j and y_k.

5. A data processing apparatus as set forth in claim 2, wherein said rules for manipulating include arithmetic operations.

6. A data processing apparatus as set forth in claim 1, wherein said processor is operative to pursue computational threads of greater and lesser probability in calculating said output information, a particular thread being terminated when its probability falls below a predetermined threshold.